PIC18F26/46/56Q71 Silicon Errata and Data Sheet Clarifications

PIC18F26/46/56Q71

Introduction

The PIC18F26/46/56Q71 devices that you have received conform functionally to the current device data sheet (DS40002329**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F26/46/56Q71 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID		
		A2	A3	A4
PIC18F26Q71	0x76E0	0xA002	0xA003	0xA004
PIC18F46Q71	0x7720	0xA002	0xA003	0xA004
PIC18F56Q71	0x7760	0xA002	0xA003	0xA004

Important: Refer to the **Device/Revision ID** section in the current **"PIC18-Q71 Family Programming Specification"** (DS40002306) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions		
				A2	A3	A4
Universal Timer Module	Level-Triggered ERS Start/Reset condition	1.1.1	Dead zone exists in level-triggered Start/Reset condition when ERS signal is generated due to an SFR access	X	X	X
	Clear Command	1.1.2	Clear command may not work properly	X		
	Interrupts	1.1.3	Interrupts do not work after leaving Debug mode	X	X	X
In-Circuit Serial Programming™	Low-Voltage Programming	1.2.1	Low-Voltage Programming is not possible when V_{DD} is below BORV while BOR is enabled	X	X	X
Electrical Specifications	Maximum Input Leakage Current	1.3.1	Increased maximum Input Leakage Current specification on 8-bit Digital-to-Analog Converter (DAC) V_{REF-} pins	X		
Universal Asynchronous Receiver Transmitter	UART	1.4.1	UART TXDE signal may go low before the Stop bit has been entirely transmitted	X	X	X
PIC18 Core	FSR Shadow Registers	1.5.1	FSR Shadow Registers are not writable	X	X	X
I^2C	Host Data Request (MDR) Bit	1.6.1	MDR bit is not cleared after Bus Time-Out	X	X	X
	Bus Time-Out	1.6.2	Bus Time-Out not detected properly when External Host Clock stretches	X	X	X
	Clock Stretch Disable	1.6.3	Clock Stretch Disable not working properly	X	X	X
	Bus Time-Out	1.6.4	Bus Time-Out causes false Start/Stop	X	X	X
	Multi-Host Mode	1.6.5	Multi-Host Mode will cause Bus failures	X	X	X
	Bus Time-Out	1.6.6	CSTR bit is not cleared after Bus Time-Out	X	X	X
	Bus Collision	1.6.7	Bus Collision followed by a Stop condition during a transaction by an external Host device may hang the bus	X	X	X
	Bus Free Time	1.6.8	I^2C - the Bus Free Divider Ratio BFREDR = 1 value is not functional	X	X	X
	Multi-Host Arbitration	1.6.9	I^2C module may hang the bus during Multi-Host Arbitration	X	X	X
CMP - Comparator	CMP	1.7.1	Comparator module will not function in ULP mode	X	X	X
Timer1	Timer1 Gate Source	1.8.1	Changing the Timer1 Gate Source may cause unexpected interrupts	X	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Universal Timer (UTMR) Module

1.1.1 Dead Zone Exists in Level-Triggered Start/Reset Condition When an ERS Signal Is Generated Due to an SFR Access

When a level-triggered Start/Reset condition (START = `'b11` or RESET = `'b01`) is triggered by an ERS signal generated by an SFR access such as TUxyPRL_Write or TUxyTMRL_Read or TUxyCRL_Read (TUxyERS = 0x3E or 0x3F), there exists a dead zone in which subsequent SFR accesses will be missed. This dead zone is the period between the ZIF flag being set and the timer starting to count again. This can be monitored by checking either the RUN status bit or the level output of the timer.

Work around

The user must wait for the timer to start counting before accessing the period, counter and capture registers again.

Affected Silicon Revisions

A2	A3	A4
X	X	X

1.1.2 Clear Command May Not Work Properly in Asynchronous Mode

When operating in asynchronous mode (CSYNC = `0`), setting the Clear Command bit (CLR= `1`) may not clear the Timer Counter register value.

Work around

Use the Universal Timer module in synchronous mode (CSYNC = `1`) when Clear Command bit (CLR) is being used.

Affected Silicon Revisions

A2	A3	A4
X		

1.1.3 Interrupts Do Not Work When Leaving Debug Mode

The Universal Timer interrupts do not work after the user exits a debug session.

Work around

Toggle the PMD bit for the corresponding instance of UTMR at the beginning of `main()` before initializing the module.

Affected Silicon Revisions

A2	A3	A4
X	X	X

1.2 Module: Low-Voltage In-Circuit Serial Programming™ (LVP)

1.2.1 Low-Voltage Programming Not Possible

Low-Voltage Programming is not possible when V_{DD} is below the selected BORV voltage level while BOR is enabled.

Work around
Method 1:

Disable BOR to use Low-Voltage Programming.

Method 2:

Raise V_{DD} above the selected BORV level while using Low-Voltage Programming.

Affected Silicon Revisions

A2	A3	A4
X	X	X

1.3 Module: Electrical Specifications

1.3.1 Increased Maximum Input Leakage Current Specification on 8-bit Digital-to-Analog Converter (DAC) V_{REF-} Pins

The 8-bit DAC V_{REF-} pins on this device have a higher sensitivity to ESD than other I/O pins. An ESD event may result in higher Leakage Current than specified (Parameter D340 in the device datasheet). This increased maximum Input Leakage Current is only applicable to the 8-bit DAC V_{REF-} pins. It is recommended that the increased ESD sensitivity on these pins be taken into consideration during design.

The table below shows the updated Input Leakage Current electrical specification on these pins:

Table 1-1. IO PORTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Device Characteristics	Min.	Typ.†	Max.	Units	Conditions
Input Leakage Current(1)							
D340	I_{IL}	I/O PORTS	—	±5	±125	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, 85°C
		I/O PORTS (for 8-bit DAC V_{REF-} pins)	**—**	**± 5**	**± 2000**	**nA**	**$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, 85°C**
D341		I/O PORTS	—	±5	±1000	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, 125°C
		I/O PORTS (for 8-bit DAC V_{REF-} pins)	**—**	**± 5**	**± 2000**	**nA**	**$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, 125°C**
D342		$\overline{MCLR}$(2)	—	±50	±200	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, 85°C

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Notes:

1. Negative current is defined as current sourced by the pin.
2. The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Work around

None.

Affected Silicon Revisions

A2	A3	A4
X		

1.4 Module: Universal Asynchronous Receiver Transmitter (UART)

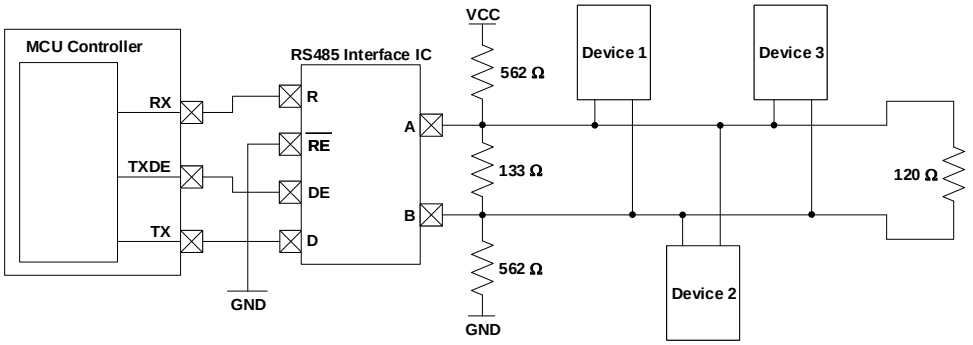
1.4.1 UART TXDE Signal May Go Low before the STOP Bit Has Been Entirely Transmitted

The UART Transmit Drive Enable (TXDE) signal could potentially transition into a low state before the UART STOP bit has been entirely transmitted due to the effects of parasitic capacitance on the TX line. In some applications, this could result in communication being prematurely terminated due to the TXDE bit going low before the STOP bit has had enough time to settle.

Work around

To ensure that the STOP bit settles into its final logic state before the TXDE signal transitions low, a biasing circuit can be implemented. A biasing circuit allows the TX line to either be driven high or low, rather than being left in a floating tri-state mode where prolonged rise or fall times could lead to communication being disrupted. This bias circuit should only be implemented on one end of the serial bus, and a termination resistor should be used on the other end. The figure below shows an example of a bias circuit that can be used to achieve this.

Please note that the resistor values used in this circuit are recommendations and that the actual resistor values required may vary based on the application.



Affected Silicon Revisions

A2	A3	A4
X	X	X

1.5 Module: PIC18 Core

1.5.1 FSR Shadow Registers Are Not Writable

Writing to the FSR Shadow Registers does not result in accurate values being stored in the registers. Consequently, reading the FSR Shadow Registers after they have been written will return inaccurate data.

Work around

Writes to the FSR shadow registers can be performed safely using the following steps:

1. Save regular FSR2 value into RAM.
2. Write the regular FSR2 with the targeted value minus the computed offset (IR[6:0] + 1, see below).

3. Write the shadow FSRxL (data doesn't matter); this will clock the shadow FSR with the FSR computed offset value.
4. Decrement FSR2 value by 1 since FSRxH increments the address by 1 (IR[6:0]).
5. Write FSRxH.
6. Restore the regular FSR2 from the stored RAM value.

The FSR shadow should have the value desired and the regular FSR should have the original value.

Affected Silicon Revisions

A2	A3	A4
X	X	X

1.6 Module: Inter-Integrated Circuit (I^2C)

1.6.1 MDR Bit Is Not Cleared after Bus Time-Out

In the Host mode of the I^2C module, when a bus time-out occurs during clock stretching and TOREC = 1, the MDR bit will not be cleared and a Stop will not be transmitted on the bus.

Work around

Force a Stop on the bus by setting the P bit upon bus time-out in Host mode. Forcing a Stop on the bus clears the MDR bit.

Affected Silicon Revisions

A2	A3	A4
X	X	X

1.6.2 Bus Time-Out Not Detected Properly When External Host Clock Stretches

When the module is operating in Client mode and an external Host device is clock stretching after the 8th SCL clock and a bus time-out occurs, the bus time-out is not detected properly. When the external Host times out before the Client and releases SCL to generate a Stop condition, the module continues to stretch SDA as if to generate an ACK and hangs the bus, and a Stop is never seen on the bus.

Work around

Reset the module by toggling the EN bit.

Affected Silicon Revisions

A2	A3	A4
X	X	X

1.6.3 Clock Stretch Disable Not Working Properly

When the CSD bit is set between a Start condition and the 8th falling SCL edge, the I^2C module enters a state where the module clock stretches indefinitely after the next Start until a bus time-out occurs.

Work around

Force a reset of the module by toggling the EN bit.

Affected Silicon Revisions

A2	A3	A4
X	X	X

1.6.4 Bus Time-Out Causes False Start/Stop

When the module is operating in Client mode and an external Host device is clock stretching and a bus time-out occurs in the Client, the Client releases SDA and goes into the idle state. After the external Host generates a Stop condition on the bus by releasing SCL, the module can erroneously drive a low pulse on the SDA line, which acts as a false Start and Stop on the bus.

Work around

None.

Affected Silicon Revisions

A2	A3	A4
X	X	X

1.6.5 Operating in Multi-Host Mode Will Cause Bus Failures

If operating in Multi-Host mode and a second host drives SDA low at the same time the Start bit is generated, the module will fail to go into Host mode but will continue to send an address and data as if it won arbitration. I2CCNT fails to decrement, and the module will remain in this state until a bus time-out occurs or the device is reset.

Work around

None.

Affected Silicon Revisions

A2	A3	A4
X	X	X

1.6.6 CSTR Bit Is Not Cleared after Bus Time-Out

When the module is operating in Client mode and TOREC = 1, and a bus time-out occurs during clock stretching, the CSTR bit will not be cleared, and the module continues to clock stretch and hang the bus.

Work around

Reset the I^2C module by toggling the EN bit.

Affected Silicon Revisions

A2	A3	A4
X	X	X

1.6.7 Bus Collision Followed by a Stop Condition during a Transaction by an External Host Device May Hang the Bus

In a Multi-Host environment, when another Host device on the bus causes a collision (BCLIF bit) and forces a Stop during a transaction, the I^2C module may not respond appropriately and hang the bus.

Work around

When a Bus Collision (BCLIF) is detected along with a Stop condition (PCIF), reset the I^2C module by toggling the EN bit.

Affected Silicon Revisions

A2	A3	A4
X	X	X

1.6.8 The Bus Free Divider Ratio BFREDR = 1 Value Is Not Functional

Setting the Bus Free Divider Ratio bit (BFREDR = 1) has no effect on the Bus Free Time Divider ratio.

Work around

Maintain BFREDR = 0 at all times.

Affected Silicon Revisions

A2	A3	A4
X	X	X

1.6.9 I²C Module May Hang the Bus During Multi-Host Arbitration

The I²C module may hang the bus in a Multi-Host environment when another Host device initiates a transaction on the bus by issuing the Start condition before the I²C module pulls down the SDA line, and the most significant bit of the address header starts with a '0' in FME=0 or FME=1 mode.

Work around

When using FME=0 or FME=1 modes, the user can choose to assign addresses such that the most significant bit of the address header starts with a '1'. Alternatively, the user can select the FME=2 mode of operation.

Affected Silicon Revisions

A2	A3	A4
X	X	X

1.7 Module: Comparator (CMP)

1.7.1 Comparator Module Will Not Function in ULP Mode

When operating in Ultra-Low Power (ULP) mode (VREGPM = 1x), the Comparator module will not function, even after enabling the peripheral.

Work around

Enable the Temperature Indicator module by setting the TSEN bit of the FVRCON register prior to enabling the Comparator module.

Affected Silicon Revisions

A2	A3	A4
X	X	

1.8 Module: Timer1

1.8.1 Changing the Timer1 Gate Source May Cause Unexpected Interrupts

When a new value is written into the Timer1 Gate Source Select (GSS) bits of the TxGATE register, the TMRxGIF interrupt flag may be set unexpectedly, and if the TMRxGIE bit is set, an unexpected interrupt will occur.

Work around

User software must clear the TMRxGIF bit immediately after writing the new value to the GSS bits.

Affected Silicon Revisions

A2	A3	A4
X	X	X

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002329**F**):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 None

There are no known data sheet clarifications as of this publication date.

3. Appendix A: Revision History

Doc Rev.	Date	Comments
C	10/2024	Added Silicon Revision A4. Added silicon errata 1.1.3, 1.6.7-1.6.9,1.7.1, and 1.8.1.
B	08/2023	Added Silicon Revision A3. Added silicon errata 1.1.2, 1.6.1-1.6.6.
A	11/2022	Initial document release. Includes silicon issues 1.1.1 (Universal Timer Module), 1.2.1 (ICSP), 1.3.1 (Electrical Specification), 1.4.1 (UART) and 1.5.1 (PIC18 CPU).

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